concentration in bulk silicon direct beneath the surface layer is 1×10^{15} atoms/cm^3 or less.

29. A silicon wafer, characterized in that the silicon wafer has a polycrystal silicon layer on one of major surfaces thereof and an increment of a boron concentration in an adjacent layer of a thickness of 1 μm adjacent to and including an interface between the polycrystal silicon layer and a single crystal silicon layer relative to a boron concentration in silicon in external contact with the adjacent layer is 1×10^{15} atoms/cm^3 or less.

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30. A silicon epitaxial wafer, characterized in that the silicon epitaxial wafer has a structure in which a polycrystal silicon layer is provided on a back surface of a single crystal silicon substrate and an increment of a boron concentration in an adjacent layer of a thickness of 1 μm adjacent to and including an interface between single crystal silicon of the substrate and the polycrystal silicon layer relative to a boron concentration in silicon of the substrate in external contact with the adjacent layer is 1×10^{15} atoms/cm^3 or less.

31. A silicon wafer, characterized in that the silicon wafer has a structure in which a CVD silicon oxide film is provided on one of major surfaces thereof and an increment of a boron concentration in a single crystal silicon adjacent layer of a thickness within 0.5 μm of an interface between the CVD silicon oxide film and the

silicon wafer relative to a boron concentration in bulk silicon in contact with the adjacent layer is 1 x 10^{15} atoms/cm^3 or less.

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32. A silicon epitaxial wafer, characterized in that the silicon epitaxial wafer has a structure in which a CVD silicon oxide film is provided on a back surface of a single crystal silicon substrate and an increment of a boron concentration in a substrate single crystal silicon adjacent layer of a thickness within 0.5 μm of an interface between the CVD silicon oxide film and the substrate relative to a boron concentration in silicon of the substrate in contact with the adjacent layer is 1 x 10^{15} atoms/cm^3 or less.

33. A silicon wafer according to claim 29, characterized in that the polycrystal layer a boron concentration in at least part of which is 5 x 10^{14} atoms/cm^3 or less is provided on a back surface of the silicon wafer.

34. A silicon epitaxial wafer according to claim 30, characterized in that the polycrystal layer a boron concentration in at least part of which is 5 x 10^{14} atoms/cm^3 or less is provided on a back surface of the single crystal silicon substrate.

35. A silicon wafer, characterized in that the silicon wafer has a structure in which a polycrystal silicon layer is provided on one major surface of a single crystal silicon layer and a CVD silicon oxide film is further provided on the polycrystal silicon layer, and an increment of a boron concentration in a first adjacent layer of a thickness of 1 μm adjacent to and including an interface between the polycrystal silicon layer and

the single crystal silicon layer relative to a boron concentration in silicon in external contact with the first adjacent layer is 1×10^{15} atoms/cm^3 or less and an increment of a boron concentration in a polycrystal silicon adjacent layer of a thickness of 0.5 μm adjacent to and including an interface between the CVD silicon oxide film and the polycrystal silicon layer relative to a boron concentration in polycrystal silicon in external contact with the polycrystal silicon adjacent layer is 1×10^{15} atoms/cm^3 or less.

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36. A silicon epitaxial wafer, characterized in that the silicon epitaxial wafer has a structure in which a polycrystal silicon layer is provided on a back surface of a substrate and a CVD silicon oxide film is further provided on the polycrystal silicon layer, and an increment of a boron concentration in a second adjacent layer of a thickness of 1 μm adjacent to and including an interface between the polycrystal silicon layer and a single crystal silicon layer relative to a boron concentration in silicon in external contact with the second adjacent layer is 1×10^{15} atoms/cm^3 or less and an increment of a boron concentration in a polycrystal silicon adjacent layer of a thickness of 0.5 μm adjacent to and including an interface between the CVD silicon oxide film and the polycrystal silicon layer relative to a boron concentration in polycrystal silicon in external contact with the polycrystal silicon adjacent layer is 1×10^{15} atoms/cm^3 or less.

37. A silicon wafer according to claim 27, characterized in that a boron concentration in the single crystal silicon bulk is 1×10^{16} atoms/cm^3 or less.

38. A silicon wafer according to claim 28, characterized in that a boron concentration in the single crystal silicon bulk is 1×10^{16} atoms/cm^3 or less.

39. A silicon wafer according to claim 29, characterized in that a boron concentration in the single crystal silicon bulk is 1×10^{16} atoms/cm^3 or less.

40. A silicon wafer according to claim 31, characterized in that a boron concentration in the single crystal silicon bulk is 1×10^{16} atoms/cm^3 or less.

41. A silicon wafer according to claim 35, characterized in that a boron concentration in the single crystal silicon bulk is 1×10^{16} atoms/cm^3 or less.

42. A silicon epitaxial wafer according to claim 30, characterized in that a boron concentration in the substrate is 1×10^{16} atoms/cm^3 or less.

43. A silicon epitaxial wafer according to claim 32, characterized in that a boron concentration in the substrate is 1×10^{16} atoms/cm^3 or less.

44. A silicon epitaxial wafer according to claim 36, characterized in that a boron concentration in the substrate is 1×10^{16} atoms/cm^3 or less.

45. A manufacturing process for a silicon wafer, characterized in that in manufacture of the silicon wafer according to claim 27, the silicon wafer is subjected to

handling such as treatment and storage in an atmosphere of a boron concentration of 15 ng/m^3 or less.

METHOD device

46. A manufacturing process for a silicon wafer, characterized in that in manufacture of the silicon wafer according to claim 28, the silicon wafer is subjected to handling such as treatment and storage in an atmosphere of a boron concentration of 15 ng/m^3 or less.

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M DEVICE

47. A manufacturing process for a silicon wafer, characterized in that in manufacture of the silicon wafer according to claim 29, the silicon wafer is subjected to handling such as treatment and storage in an atmosphere of a boron concentration of 15 ng/m^3 or less.

M DEVICE

48. A manufacturing process for a silicon wafer, characterized in that in manufacture of the silicon wafer according to claim 31, the silicon wafer is subjected to handling such as treatment and storage in an atmosphere of a boron concentration of 15 ng/m^3 or less.

M D

49. A manufacturing process for a silicon wafer, characterized in that in manufacture of the silicon wafer according to claim 35, the silicon wafer is subjected to handling such as treatment and storage in an atmosphere of a boron concentration of 15 ng/m^3 or less.

M D

50. A manufacturing process for a silicon epitaxial wafer, characterized in that in manufacture of the silicon epitaxial wafer according to claim 30, the silicon epitaxial wafer is subjected to handling such as treatment and storage in an atmosphere of a boron concentration of 15 ng/m^3 or less.

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M D

51. A manufacturing process for a silicon epitaxial wafer, characterized in that in manufacture of the silicon epitaxial wafer according to claim 32, the silicon epitaxial wafer is subjected to handling such as treatment and storage in an atmosphere of a boron concentration of 15 ng/m^3 or less.

M D

52. A manufacturing process for a silicon epitaxial wafer, characterized in that in manufacture of the silicon epitaxial wafer according to claim 36, the silicon epitaxial wafer is subjected to handling such as treatment and storage in an atmosphere of a boron concentration of 15 ng/m^3 or less.

M D

53. A manufacturing process for a silicon wafer, characterized in that in manufacture of the silicon wafer according to claim 29, formation of a polycrystal silicon layer is performed in an atmosphere of a boron concentration of 15 ng/m^3 or less.

M D

54. A manufacturing process for a silicon wafer, characterized in that in manufacture of the silicon wafer according to claim 35, formation of a polycrystal silicon layer is performed in an atmosphere of a boron concentration of 15 ng/m^3 or less.

55. A manufacturing process for a silicon epitaxial wafer, characterized in that in manufacture of the silicon epitaxial wafer according to claim 30, formation of a polycrystal silicon layer is performed in an atmosphere of a boron concentration of 15 ng/m^3 or less.

56. A manufacturing process for a silicon epitaxial wafer, characterized in that in manufacture of the silicon epitaxial wafer according to claim 36, formation of a polycrystal silicon layer is performed in an atmosphere of a boron concentration of 15 ng/m^3 or less.

57. A manufacturing process for a silicon wafer, characterized in that in manufacture of the silicon wafer according to claim 31, formation of a CVD silicon oxide film is performed in an atmosphere of a boron concentration of 15 ng/m^3 or less.

58. A manufacturing process for a silicon wafer, characterized in that in manufacture of the silicon wafer according to claim 35, formation of a CVD silicon oxide film is performed in an atmosphere of a boron concentration of 15 ng/m^3 or less.

59. A manufacturing process for a silicon epitaxial wafer, characterized in that in manufacture of the silicon epitaxial wafer according to claim 30, formation of a CVD silicon oxide film is performed in an atmosphere of a boron concentration of 15 ng/m^3 or less.

60. A manufacturing process for a silicon epitaxial wafer, characterized in that in manufacture of the silicon epitaxial wafer according to claim 36, formation of a CVD silicon oxide film is performed in an atmosphere of a boron concentration of 15 ng/m^3 or less.

61. A manufacturing process for a silicon wafer, characterized in that in manufacture of the silicon wafer according to claim 29, a polycrystal layer is formed on a surface on which an attached boron amount is suppressed to 1 x 10^{10} atoms/cm^2 or less.

62. A manufacturing process for a silicon wafer, characterized in that in manufacture of the silicon wafer according to claim 35, a polycrystal layer is formed on a surface on which an attached boron amount is suppressed to 1 x 10^{10} atoms/cm^2 or less.

63. A manufacturing process for a silicon epitaxial wafer, characterized in that the manufacture of the silicon epitaxial wafer according to claim 30, a polycrystal layer is formed on a surface on which an attached boron amount is suppressed to 1 x 10^{10} atoms/cm^2 or less.

64. A manufacturing process for a silicon epitaxial wafer, characterized in that the manufacture of the silicon epitaxial wafer according to claim 36, a polycrystal layer

is formed on a surface on which an attached boron amount is suppressed to 1×10^{10} atoms/cm^2 or less.

A 65. An atmosphere control apparatus, characterized in that the atmosphere control apparatus controls a boron concentration in an atmosphere to be 15 ng/m^3 or less.

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A 66. A clean room, characterized in that a boron concentration in an atmosphere of the clean room is 15 ng/m^3 or less.

A 67. Clean room air conditioning facilities comprising: an air conditioner having a boron-less filter and a boron adsorbing filter; and one or more of wafer treatment apparatuses each having a boron-less filter, wherein an atmosphere gas is recycled between the air conditioner, the clean room and the wafer treatment apparatuses.

68. Clean room air conditioning facilities according to claim 67, having a boron-less filter and a boron adsorbing filter.

69. Clean room air conditioning facilities according to claim 67, in which an internal pressure of a wafer treatment apparatus is adjusted to be higher than a clean room internal pressure and the clean room internal pressure is adjusted to be higher than an external pressure.

70. A manufacturing process for a wafer, characterized in that manufacture of the wafer is performed using clean room air conditioning facilities according to claim 67, the wafer being characterized in that an attached boron amount on a surface of the silicon wafer is 1×10^{10} atoms/cm^2 or less.

71. A manufacturing process for a wafer, characterized in that manufacture of the wafer is performed using clean room air conditioning facilities according to claim 67, the wafer being characterized in that an increment of a boron concentration in a surface layer down to a depth of 0.5 μm relative to a boron concentration in bulk silicon direct beneath the surface layer is 1×10^{15} atoms/cm^3 or less. .

72. A manufacturing process for a wafer, characterized in that manufacture of the wafer is performed using clean room air conditioning facilities according to claim 67, the wafer being characterized in that the silicon wafer has a polycrystal silicon layer on one of major surfaces thereof and an increment of a boron concentration in an adjacent layer of a thickness of 1 μm adjacent to and including an interface between the polycrystal silicon layer and a single crystal silicon layer relative to a boron concentration in silicon in external contact with the adjacent layer is 1×10^{15} atoms/cm^3 or less.

73. A manufacturing process for a wafer, characterized in that manufacture of the wafer is performed using clean room air conditioning facilities according to claim 67, the wafer being characterized in that the silicon epitaxial wafer has a structure in which

a polycrystal silicon layer is provided on a back surface of a single crystal silicon substrate and an increment of a boron concentration in an adjacent layer of a thickness of 1 μm adjacent to and including an interface between single crystal silicon of the substrate and the polycrystal silicon layer relative to a boron concentration in silicon of the substrate in external contact with the adjacent layer is 1×10^{15} atoms/cm^3 or less.

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74. A manufacturing process for a wafer, characterized in that manufacture of the wafer is performed using clean room air conditioning facilities according to claim 67, the wafer being characterized in that the silicon wafer has a structure in which a CVD silicon oxide film is provided on one of major surfaces thereof and an increment of a boron concentration in a single crystal silicon adjacent layer of a thickness within 0.5 μm of an interface between the CVD silicon oxide film and the silicon wafer relative to a boron concentration in bulk silicon in contact with the adjacent layer is 1×10^{15} atoms/cm^3 or less.

75. A manufacturing process for a wafer, characterized in that manufacture of the wafer is performed using clean room air conditioning facilities according to claim 67, the wafer being characterized in that the silicon epitaxial wafer has a structure in which a CVD silicon oxide film is provided on a back surface of a single crystal silicon substrate and an increment of a boron concentration in a substrate single crystal silicon adjacent layer of a thickness within 0.5 μm of an interface between the CVD silicon oxide film and the substrate relative to a boron concentration in silicon of the substrate in contact with the adjacent layer is 1×10^{15} atoms/cm^3 or less.

76. A manufacturing process for a wafer, characterized in that manufacture of the wafer is performed using clean room air conditioning facilities according to claim 67, the wafer being characterized in that the silicon wafer has a structure in which a polycrystal silicon layer is provided on one major surface of a single crystal silicon layer and a CVD silicon oxide film is further provided on the polycrystal silicon layer, and an increment of a boron concentration in a first adjacent layer of a thickness of 1 μm adjacent to and including an interface between the polycrystal silicon layer and the single crystal silicon layer relative to a boron concentration in silicon in external contact with the first adjacent layer is 1×10^{15} atoms/cm^3 or less and an increment of a boron concentration in a polycrystal silicon adjacent layer of a thickness of 0.5 μm adjacent to and including an interface between the CVD silicon oxide film and the polycrystal silicon layer relative to a boron concentration in polycrystal silicon in external contact with the polycrystal silicon adjacent layer is 1×10^{15} atoms/cm^3 or less.

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77. A manufacturing process for a wafer, characterized in that manufacture of the wafer is performed using clean room air conditioning facilities according to claim 67, the wafer being characterized in that the silicon epitaxial wafer has a structure in which a polycrystal silicon layer is provided on a back surface of a substrate and a CVD silicon oxide film is further provided on the polycrystal silicon layer, and an increment of a boron concentration in a second adjacent layer of a thickness of 1 μm adjacent to and including an interface between the polycrystal silicon layer and a single crystal silicon layer relative to a boron concentration in silicon in external contact with the second